Application Number: 09/694,176 Docket: 98-15DIV1

## AMENDMENTS TO THE SPECIFICATION

Please substitute the following replacement paragraph(s) for the previously-pending versions of such paragraph(s). The replacement paragraph(s) are marked-up to show changes from the previously-pending versions thereof. Please add the following new paragraph(s) as indicated.

*** Replace the paragraph at page 1, lines 9-11 with the following replacement paragraph:

This application is a divisional of U.S. application No. 09/119,187 filed on July 20, 1998, now U.S. patent No. 6,187,164, which itself is a continuation-in-part of U.S. application No. 08/941,170 filed September 30, 1997, ~~pending~~ now abandoned, the techniques of each of which are incorporated herein by reference for all purposes.

*** Please replace the paragraph at page 5, line 27 through page 6, line 6 with the following replacement paragraph:

Still referring to FIGS. 1A and 1B, a patterned insulating layer 18 covers the wires 16 and an inner portion of the peripheral contact pads 13, but leaves the electrodes 12 and the outer portion of the peripheral contact pads 13 exposed (preferably approximately half of the ~~contract~~ contact pad 13 is covered with this insulating layer). Because of the insulating layer 18, it is possible to connect a lead (e.g., an alligator clip) to the outer portion of a given contact pad 13 and address its associated electrode 12 while the array 10 is immersed in solution, without having to worry about reactions that can occur on the wires 16 or peripheral contact pads 13. The insulating layer 18 may be, for example, glass, silica ($SiO_2$), alumina ($Al_2O_3$), magnesium

oxide (MgO), silicon nitride ($Si_3N_4$), boron nitride (BN), yttrium oxide ($Y_2O_3$), titanium dioxide ($TiO_2$), hardened photoresist, or other suitable material known to be insulating in nature.

*** Replace the paragraph at page 6, line 28 through page 7, line 20 with the following replacement paragraph:

A primary electrode mask 27, an example of which is shown in Fig. 2B, (which is the negative of the electrode array pattern desired) is then placed over the wafer that is then photolyzed on a mask aligner system (commonly used and familiar to those skilled in the art). After exposure to ultraviolet (UV) light during the photolysis step 26, regions 29 on the wafer are then dissolved away using an appropriate developing solution (e.g., Shipley Microposit MF-319 or equivalent). The wafer is then placed in a physical vapor deposition (PVD) system where a metals are deposited during a metal deposition step 28. Example PVD systems include: sputtering, electron beam evaporation and pulsed laser deposition. The metals deposited by the appropriate PVD system consist of an adhesion layer (such as Cr, Ta, or W) followed by the desired electrode material (such as Au, Ag, Cu or Pt). The thicknesses of these layers may vary substantially, but are typically 100-500 Å for the adhesion layer and 1000-5000 Å for the electrode layer. Following a lift-off step 30 to remove the excess metals, a second layer of photoresist is then deposited on the wafer during a second photoresist deposition step 32, cured as described above, and photolyzed through an isolation mask 35 during a second photolysis step 34. The aim of this second photolysis step is to expose only the regions of the electrode pads 36 and an outer contact ring 38, the exposed photoresist on which is dissolved away after the photolysis step. A final annealing step 40 at between 90°C and 130°C for between 1 minute and 10 (or more) minutes hardens the remaining photoresist into an effective insulating layer.

Alternately, an insulating layer (such as glass, silica, alumina, magnesium oxide, silicon nitride, boron nitride, yttrium oxide or titanium dioxide) may be deposited in place of the hardened photoresist by a suitable PVD technique after photolysis of the second photoresist layer through an inverse isolation mask (the negative of the isolation mask 35 in Fig. 2C).

*** Replace the paragraph at page 11, lines 11-17 with the following replacement paragraph:

Using the PCB 112 in conjunction with the deposition head 50 (Fig. 3) and the multi-channel potentiostat, each individual electrode on a given anode array can be individually addressed (e.g., during an electrodeposition procedure). Alternatively, using the PCB in connection with the electrochemical cell setup 80 (Fig. 4A) and multi-channel potentiostat, all of the electrodes on the array ~~may~~ may be simultaneously addressed (e.g., during a catalytic activity measurement). Such catalytic measurements can be made in a time frame of between 1 and 2 minutes for each array of materials.

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**[NO FURTHER AMENDMENTS THIS PAGE]**